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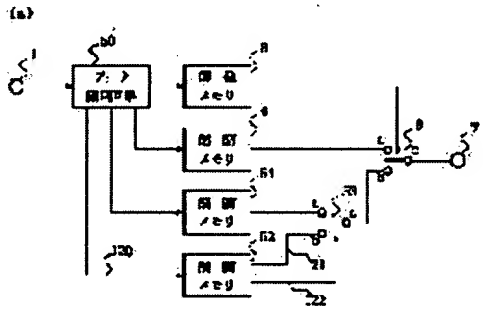
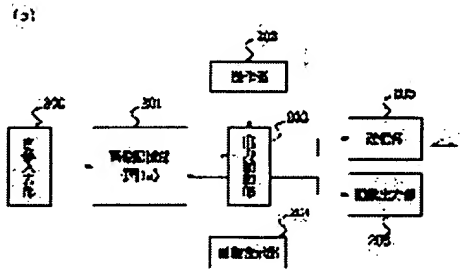
(54) IMAGE PROCESSOR

(57)Abstract:

PROBLEM TO BE SOLVED: To efficiently express images for which color line images and halftone images coexist with high image quality by turning bit map data for indicating the line images, the coloring data and image data for indicating the halftone images into the image data for constituting one screen.

SOLUTION: For data inputted from the input terminal 1 of an image storage part 201, header information is interpreted in a data identification circuit 50, the bit map data of a text are stored in a resolution memory 3, the gradation (color) data of the text are stored in a gradation memory 4, a background color is stored in the gradation memory 51, and the image data provided with a halftone are stored in the gradation memory 52 respectively. The read of the memories is controlled, so as to output the data corresponding to respective pixels successively from the head of a page from the resolution memory 3 and the gradation memories 4, 51 and 52 corresponding to synchronization signals from a printer side. To the control terminal of a selector 53, image area signals 122 outputted from the gradation memory 52 are inputted. The data for the changeover of the gradation memories 4 and 5 are 1-bit data for holding a resolution stored in the resolution memory 3.





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CLAIMS

[Claim(s)]
[Claim 1] The bit map data in which a line drawing image is shown, and the staining data expressing the color of said bit map data, A generating means to generate the image data which shows a halftone image as image data for constituting one screen, The 1st output means which outputs the bit map data generated with said generating means, The image processing system characterized by having the 2nd output means which carries out lossy compression of the staining data generated with said generating means, and outputs them, and the 3rd output means which carries out lossy compression of the image data generated with said generating means, and outputs it.
[Claim 2] The resolution which the staining data outputted by said 2nd output means express is an image processing system according to claim 1 characterized by being restricted lower than the resolution which the bit map data outputted by said 1st output means express.
[Claim 3] Said 3rd output means is an image processing system according to claim 1 characterized by carrying out JPEG coding of said image data.
[Claim 4] Said generating means is an image processing system according to claim 1 characterized by generating the background color data expressing a background color as data for constituting said one screen.
[Claim 5] Said bit map data are an image processing system according to claim 1 characterized by expressing by 1 bit of each pixel.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the image processing system for memory-storing or transmitting efficiently, the image data which shows a color picture.
[0002]
[Description of the Prior Art] It will be classified into color line drawings, such as a color alphabetic character and a color graphic, and halftone images, such as a photograph, if a color picture is generally roughly classified.
[0003] As for a monochrome line drawing, being expressed with high resolution is desirable. However, in the case of this color line drawing, the tint of a line drawing itself does not need resolution so much. On the other hand, as for a halftone image, being expressed in the Takashina tone is desirable.
[0004]
[Problem(s) to be Solved by the Invention] However, the approach of compressing efficiently a color picture in which a color line drawing and a halftone image are intermingled was not yet established conventionally.
[0005] This invention is accomplished in view of the above-mentioned conventional example, and it aims at expressing a high definition image especially using this image data for the purpose of offering the configuration of the image data which expresses efficiently an image with which a color line drawing and a halftone image are intermingled.
[0006]
[Means for Solving the Problem] The bit map data in which a line drawing image is shown according to the image processing system of this invention in order to solve an above-mentioned technical problem, A generating means to generate the staining data expressing the color of said bit map data, and the image data which shows a halftone image as image data for constituting one screen, The 1st output means which outputs the bit map data generated with said generating means, It is characterized by having the 2nd output means which carries out lossy compression of the staining data generated with said generating means, and outputs them, and the 3rd output means which carries out lossy compression of the image data generated with said generating means, and outputs it.
[0007] It is characterized by making it lower than the resolution as which the bit map data outputted by said 1st output means express the resolution which the staining data especially outputted by said 2nd output means express.
[0008]
[Embodiment of the Invention]
(Gestalt of the 1st operation) Drawing 1 (a) is the block diagram showing the configuration of the image storage section of the image processing system concerning the gestalt of operation of the 1st of this invention. As for gradation memory, and 6 and 53, for resolving memory and 50, a data discrimination decision circuit, and 4, 51 and 52 are [one / an input terminal and 3 / a selector and 7] output terminals among drawing.

[0009] As for the data which the host computer etc. is connected to the input terminal 1, and were inputted from the input terminal 1, header information is interpreted by the data discrimination decision circuit 50, and the image data to which, as for a background color, the gradation (color) data of a text have halftone in the gradation memory 51 at the gradation memory 4 is respectively stored in the resolving memory 3 for the bit map data of a text at the gradation memory 52. If the data for 1 page are transmitted to each above-mentioned memory from a host computer and printer engine is started, according to the synchronizing signal from a printer side, read-out of memory will be controlled so that the data corresponding to each pixel are outputted to order by the head of a page from the resolving memory 3 and the gradation memory 4, 51, and 52. The image field signal 122 which the output (namely, background color) of the gradation memory 51 is connected to the terminal a of a selector 53, and the output (namely, image data) 121 of the gradation memory 52 is connected to Terminal b, and is outputted to a control terminal from the gradation memory 52 is inputted. Therefore, when the present pixel is an image field, out of an image field, a background color is outputted for an image data to the terminal c of a selector 52 (the terminal b of a selector 6 is supplied).
[0010] According to the output data of the resolving memory 3, when the data of the resolving memory 3 are "1" and the data of the resolving memory 3 are "0" about the data (namely, data of the gradation memory 4) of Terminal a as a drawing color, a selector 6 chooses the data (namely, data of the gradation memory 5) of Terminal b as a background color, and outputs gradation data to printer engine from an output terminal 7.
[0011] The data stored in the resolving memory 3 are data for the gradation memory 4 and the change of five, and are data of 1 bit of each pixel by this example for resolution maintenance.
[0012] On the other hand, although full gradation data (a total of 24-bit data [The gestalt of this operation] of 8 bits each of RGB) are respectively stored in the gradation memory 4 and 51, the number of pixels (resolution) is restricted for memory space reduction.
[0013] Drawing 2 is the block diagram showing the example of a concrete configuration of the gradation memory 52 of the gestalt of this operation. For memory and 54, as for a compression circuit and 56, a compressibility setting circuit and 55 are [nine / an expanding circuit and 57] field detectors among drawing.
[0014] The start address and the image area size, i.e., the width of face, and the height of an image field are set to the header of an image data, and from the width of face and the height of the above-mentioned image field, in quest of the amount of data of an image field, the compressibility setting circuit 54 sets up compressibility from a ratio with the capacity of memory 9, and outputs it to the compression circuit 55. The compression circuit 55 is a circuit as shown in drawing 3 , quantization conditions are controlled to become the set-up compressibility and compressed data is stored in memory 9. Moreover, in the compressibility setting circuit 54, from header information, the coordinate value of the starting point of an image field and a terminal point is also generated, and the above-mentioned coordinate value is set as each register of the field detector 57. The field detectors 57 are the field detector 33 of drawing 7 mentioned later, and same circuit.
[0015] On the other hand, synchronizing with HSYNC by the side of a printer, if printer engine is started, the field detector 57 will output an image field signal from a signal line 122, when the present pixel judges whether it is the pixel of an image field and judges with an image field. If an image field signal is inputted into the expanding circuit 56, the expanding circuit 56 will elongate the compressed data stored in memory 9 to the original image data, and will output it from a signal line 121.
[0016] The compression circuit 55 is a compression coding network which performs well-known coding of orthogonal transformation coding, vector quantization, block coding, etc. With the gestalt of this operation, for memory space reduction, since the compression ratio is set up quite highly, irreversible coding is used. Therefore, resolution is not saved. However, of course, reversible coding, such as run length coding, may be used.
[0017] Drawing 3 is the block diagram showing the example of a concrete configuration of the compression circuit 55. The gestalt of this operation is Baseline of the international-standards-ized proposal of color static-image coding proposed in JPEG (Joint Photographic Expert Group) which is the

joint activity object of ISO and CCITT. The coding section of System is shown. (407 Bibliography: Yasuda, "formation of color still picture coding international standards", the Institute of Image Electronics Engineers of Japan, the 18th volume, No. 6, PP.398- 1989)

[0018] The image pixel data inputted from the signal line 103 are cut down 8x8 pixels in the shape of a block in the blocking circuit 11 constituted by the Rhine memory for several lines, cosine conversion is carried out in the discrete cosine transform (DCT) circuit 12, and a transform coefficient is supplied to a quantizer (Q) 13. In a quantizer 13, linear quantization of a transform coefficient is performed according to the quantization step information impressed on the quantization table 14. Among the quantized transform coefficients, difference (prediction error) with DC component of a pre-block is taken in the predicting-coding circuit (DPCM) 15, and DC multiplier is supplied to the Huffman coding circuit 16. Drawing 4 is the detailed block block diagram of the predicting-coding circuit 15. DC multiplier quantized from the quantizer 13 is impressed to a delay circuit 25 and a subtractor 216. A delay circuit 25 is a circuit delayed by the time amount which needs a discrete cosine transform circuit for 1 block, i.e., the operation for 8x8 pixels, therefore DC multiplier of a pre-block is supplied to a subtractor 26 from a delay circuit 25. Therefore, the difference (prediction error) of DC multiplier with a pre-block will be outputted to the output of a subtractor 26. (Since the pre-block value is used as a forecast, a prediction machine consists of these predicting coding like the above-mentioned in a delay circuit.)

[0019] The Huffman coding circuit 16 carries out variable length coding of the prediction error signal supplied from the predicting-coding circuit 15 according to DC Huffman code table 17, and supplies DC Huffman code to the multiplexing circuit 24.

[0020] On the other hand, as the scanning conversion circuit 18 shows to drawing 5 (a) from the multiplier of a low degree, the zigzag scan of the AC multiplier (multipliers other than DC multiplier) quantized with the quantizer 13 is carried out at order, and it is supplied to the capable multiplier detector 19. Quantized AC multiplier judges whether it is "0", in the case of "0", a count-up signal is supplied to the run length counter 20, and it makes the value of a counter increase +one time in the capable multiplier detector 19. On the other hand, in the case of multipliers other than "0", a reset signal is supplied to a run length counter, while resetting the value of a counter, a multiplier is divided into group number SSSS and an overhead bit as shown to drawing 5 (b) by the grouping circuit 21, group number SSSS is supplied to the Huffman coding circuit 22, and an overhead bit is respectively supplied to the multiplexing circuit 24. The run length counter 20 supplies the number NNNN of "0" between capable multipliers other than "0" to the Huffman coding circuit 22 in the circuit which counts the run length of "0." The Huffman coding circuit 22 carries out variable length coding of the group number SSSS of a capable multiplier to the run length NNNN of supplied "0" according to AC Huffman code table 23, and supplies AC Huffman code to the multiplexing circuit 24.

[0021] In the multiplexing circuit 24, DC Huffman code, AC Huffman code, and the overhead bit for 1 block (input pixel of 8x8) are multiplexed, and the image data compressed from the signal line 104 is outputted.

[0022] Therefore, the compressed data outputted from a signal line 104 is memorized in memory, and reduction of memory space is possible for the time of above-mentioned compression at the time of read-out by elongating by reverse actuation.

[0023] In addition, since the expanding circuit 56 performs the twist operations of the compression circuit 8, explanation is omitted.

[0024] Drawing 6 is the block diagram showing the concrete example of a configuration of the gradation memory 4 and 51. As for a selector and 30, 29 and 31 are [a register group and 32] field judging circuits among drawing.

[0025] Sequential storing of the gradation data inputted from the signal line 108 is carried out by the selector 29 from a register 30-2 to 30-n. In addition, default gradation data (for example, the gradation memory 4 white and the gradation memory 51 white) are set to the register 30-1. The field judging circuit 32 judges the range where the gradation data stored in each register become effective from the coordinate value of the output data of the resolving memory 3 inputted from a signal line 105,106, controls a selector 31, and outputs effective gradation data from a signal line 109.

[0026] Drawing 7 is the block diagram showing the concrete example of a configuration of the field judging circuit 32. As for a register, and 39 and 40, for a field detector and 34, a priority encoder, and 35, 36, 37 and 38 are [33 / a comparator circuit and 41] AND circuits among drawing.
[0027] With the gestalt of this operation, it limits to a rectangle as shows the service area of each gradation register 30-2 - 30-n to drawing 8 , and sets up by two of the points (x1, y1) (a "terminal point" is called a rectangular lower right corner and the following among drawing) scanned by the point (x0, y0) (the "starting point" is called the rectangular upper-left-hand-corner section and the following among drawing 8) scanned first, and the last. In addition, the direction of the x axis in drawing is made into the main scanning direction of a printer, and the direction of the y-axis is made into the direction of vertical scanning. the coordinate value (x0, y0) of the above-mentioned starting point identified from the data discrimination decision circuit 2 and a terminal point, and (x1, y1) are stored in the each registers 35, 37, 36, and 38 of the field detector 33 corresponding to the gradation register 30 of drawing 6 .
[0028] On the other hand, at the time of print-out, each coordinate value of the pixel data read from the resolving memory 3 is inputted from a signal line 105,106. The 1st comparator circuit 39 compares the x-coordinate value x of the above-mentioned resolving memory 3 with the x-coordinate values x0 and x1 of the starting point and x terminal points, and inputs "0" into AND circuit 41 for "1" at the time of x<x0 or x>x1 at the time of x0 <=x<=x1. The 2nd comparator circuit 40 inputs "0" into AND circuit 41 for "1" similarly at the time of y<y0 or y>y1 at the time of y0 <=y<=y1. Therefore, "0" is outputted at the times other than "1", and (ii) and (i) at the time of (i) x0 <=x<=x1 and y0 <=y<=y1, and field detection is attained from AND circuit 41. By the priority encoder 34, the number of the field set as the last among the detected fields is encoded, and the result detected in each field detector 33-2 - 33-n is outputted from a signal line 107, in order to perform the priority judging of a duplication part as shown in the slash section of drawing 8 . That is, in a duplication part, it is judged with the field set up later being effective. In addition, when each field judging results of all are set to "0", a priority encoder 34 outputs "0" and controls a selector 31 to choose the gradation data (namely, default) of the gradation register 30-1 of drawing 6 .
[0029] Usually, the dot resolving data with which high resolutions, such as a text, are demanded are stored in the resolving memory 3, and the data with which the Takashina tonality, such as an image, is demanded are stored in the gradation memory 5. The gradation (color) data of text data are stored in the gradation memory 4. When the text data to which the case of regularity (namely, monochrome) or a background (background color) laps [the gradation (color) of text data] with the image section in regularity (monochrome) over 1 page is the above-mentioned background color, since the contents of the above and the gradation memory 4 serve as only a default, they become unnecessary [the register after said field judging circuit 32 and 30-2].
[0030] In addition, a configuration which carries out 1 gradation (color) setup per block of 8 (pixel)x8 (Rhine) is sufficient as gradation memory.
[0031] Although the resolving memory 3 is memory which has the capacity for a page by 1 bit of each pixel, since it is used for the change of gradation data, the correlation between pixels is quite high and compression of the amount of data is also possible by using reversible data compression coding as shown in drawing 12 .
[0032] Drawing 12 is the block diagram showing the gestalt of other operations of the resolving memory 3. For a run-length-coding circuit and 61, as for memory and 63, a Huffman coding circuit and 62 are [60 / the Huffman decryption circuit and 64] run length decryption circuits among drawing. Since it is well-known about a run length, and Huffman coding and a decryption circuit, explanation is omitted.
[0033] Drawing 1 (b) is drawing containing the image storage section of drawing 1 (a) showing the whole image processing system configuration.
[0034] In drawing 1 (b), although 200 is the image input section connected with the host computer, you may be the interface of external instruments, such as image readers, such as an image scanner containing a CCD sensor, and SV camera, a video camera, etc. In the case of the latter, in the data discrimination decision circuit 50, it is made to identify the above-mentioned data. The image data inputted from 200 is supplied to the input terminal 1 of the image storage section 201 shown in drawing 1 (a). The control

unit to which, as for 202, an operator performs assignment of the output destination change of image data etc., and 203 are the output-control sections, and perform the output of the synchronizing signal of memory read-out, such as selection of the output destination change of image data, and HSYNC of printer engine, etc. A synchronizing signal is supplied to the discrimination decision circuit 50 and each memory of drawing 1 (a), and is used as control signals, such as read-out from a data transfer and memory. The transmitting section which 204 minds the image display sections, such as a display, and 205 minds a public line and a Local Area Network, and communicates image data, and 206 are the image output sections, such as a laser beam printer which irradiates a laser beam, forms a latent image for example, on a photo conductor, and visible-image-izes this. In addition, the image output sections 206 may be an ink jet printer, a thermal transfer printer, a dot impact printer, etc.

[0035] As mentioned above, the image memory which the gestalt of this operation compresses continuous tone data, such as an image data, using the correlation between pixels, and a vision property, and is memorized, The gradation memory which memorizes a text color (drawing color) or a background color for every specific region, Reduction of memory space is aimed at keeping good the image quality of both a text and an image by preparing the resolving memory which saves the dot resolution of pixel data, and switching the output data of the above-mentioned image memory and gradation memory according to the output signal of this resolving memory.

[0036] (Gestalt of the 2nd operation) Drawing 9 is the block diagram showing the configuration of the image processing system concerning the gestalt of operation of the 2nd of this invention. The same coding is given to the component which achieves the same function as drawing 1 among drawing, and only a different point from the gestalt of operation of drawing 1 is explained hereafter.

[0037] It is 2 bundle data discrimination decision circuit among drawing. As for the data inputted from the input terminal 1, header information is interpreted in the data discrimination decision circuit 44, a drawing color [in / to the resolving memory 3 / in the resolving data for background discernment / a background color and an image field] is stored in the gradation memory 4, and the drawing color and image data of a text are respectively stored in the gradation memory 52. If the data for 1 page are transmitted to each above-mentioned memory 3, 4, and 52 and printer engine is started, from the resolving memory 3 and the gradation memory 4 and 52, the data corresponding to each pixel will be respectively supplied to the control terminal of a selector 6, Terminal a, and Terminal b one by one from the head pixel of a page by the synchronizing signal. A selector 6 outputs gradation data for the background color which is the output of the gradation memory 4, the drawing color of the text which is the output of the gradation memory 52, and an image data to printer engine from a change and an output terminal 7 according to the output signal of the resolving memory 3.

[0038] It consists of gestalten of this operation so that the resolution of a background may be saved. Usually, to the drawing color number of a text, since it is very few, the hard amount of the gradation memory 4 can do the background color number in 1 page quite small. Moreover, by the gestalt of the 1st operation, when the drawing color of a text changes continuously (in the name case [For example, the gradation and the coordinate of an alphabetic character were shifted little by little, and carried out overwrite. it needs.]), although false gradation processing of a dither etc. is actually needed, with the gestalt of this operation, very good image quality is acquired by storing said drawing color in the gradation memory 5 advantageous to storage of a continuous tone. Moreover, since it consists of gestalten of this operation so that the resolving power of a background may be saved, trimming of the image section can be easily performed by the maximum resolution of a printer.

[0039] (Gestalt of the 3rd operation) Drawing 10 is the block diagram showing the configuration of the image-processing store concerning the gestalt of operation of the 3rd of this invention. The same sign is given to the component which achieves the same function as drawing 1 among drawing, and only a different point from the gestalt of operation of drawing 1 is explained hereafter.

[0040] As for a data discrimination decision circuit and 45, 44 are [a field judging circuit and 46] EXOR circuits among drawing.

[0041] As for the data inputted from the input terminal 1, header information is interpreted in the data discrimination decision circuit 44, a drawing color [in / to the resolving memory 3 / in the bit map data

of a background / a background color and an image field] is stored in the gradation memory 4, and the drawing color and image data of a text are respectively stored in the gradation memory 52. Moreover, an image field is stored in the register of the field judging circuit 45. The data for 1 page are transmitted to each above-mentioned memory 3, 4, and 52 from a host computer, and if printer engine is started, from the resolving memory 3, the gradation memory 4 and 52, and the field judging circuit 45, the data corresponding to each pixel will be outputted one by one from the head pixel of a page. The field judging circuit 45 supplies "1" to one terminal of the EXOR circuit 46, when the present pixel is an image data. The output of the resolving memory 3 is connected to another terminal of the EXOR circuit 46, and the resolving data in an image field are reversed by the above-mentioned configuration. Therefore, as for a selector 6, in the case of the text pixel in a background and an image field, the gradation data which outputted the gradation (color) data of a terminal b 5, i.e., gradation memory, from Terminal c except the above, and were chosen from the output terminal 7 are supplied to printer engine in the gradation (color) data of a terminal a 4, i.e., gradation memory.

[0042] With the gestalt of this operation, since the contents of resolving memory are reversed in the image section, overwrite of text data can perform easily. That is, process the text data which carries out overwrite to the above-mentioned image section with a host computer as background data with the gestalt of the 2nd operation. That is, with the gestalt of this operation, although it is necessary in "1" to store "0" in addition to the above, only the image section by which overwrite of the text is not carried out to the resolving memory 3, and the text drawing section outside an image field should always set the text drawing section as "1" irrespective of the inside and outside of an image field in order to reverse the output of the resolving memory 3 in an image field.

[0043] In addition, although resolving memory was constituted from 1 bit of each pixel in the gestalt of the 1st - the 3rd operation, this invention is good also as a configuration which chooses gradation data from four kinds of gradation memory as 2 bits not only of this but each pixel.

[0044]

[Effect of the Invention] While being able to express efficiently an image with which a color line drawing and a halftone image are intermingled since the bit map data which were explained above, and in which a line drawing image is shown according to [like] this invention, the staining data expressing the color of said bit map data, and the image data which shows a halftone image are made into the image data for constituting one screen, among these lossy compression of staining data and the image data is carried out and it outputs, a high definition image can be expressed using these image data.

[0045] Image quality is also maintainable while being able to control the total amount of signs, since degradation of image quality carries out lossy compression to few above-mentioned staining data and image datas even if it carries out data reduction comparatively when bit map data, the staining data expressing the color of bit map data, and the image data that shows a halftone image specifically express an image as mentioned above.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the image processing system for memory-storing or transmitting efficiently, the image data which shows a color picture.

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PRIOR ART

[Description of the Prior Art] It will be classified into color line drawings, such as a color alphabetic character and a color graphic, and halftone images, such as a photograph, if a color picture is generally roughly classified.
[0003] As for a monochrome line drawing, being expressed with high resolution is desirable. However, in the case of this color line drawing, the tint of a line drawing itself does not need resolution so much. On the other hand, as for a halftone image, being expressed in the Takashina tone is desirable.

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EFFECT OF THE INVENTION

[Effect of the Invention] While being able to express efficiently an image with which a color line drawing and a halftone image are intermingled since the bit map data which were explained above, and in which a line drawing image is shown according to [like] this invention, the staining data expressing the color of said bit map data, and the image data which shows a halftone image are made into the image data for constituting one screen, among these lossy compression of staining data and the image data is carried out and it outputs, a high definition image can be expressed using these image data.
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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the approach of compressing efficiently a color picture in which a color line drawing and a halftone image are intermingled was not yet established conventionally.
[0005] This invention is accomplished in view of the above-mentioned conventional example, and it aims at expressing a high definition image especially using this image data for the purpose of offering the configuration of the image data which expresses efficiently an image with which a color line drawing and a halftone image are intermingled.
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MEANS

[Means for Solving the Problem] The bit map data in which a line drawing image is shown according to the image processing system of this invention in order to solve an above-mentioned technical problem, A generating means to generate the staining data expressing the color of said bit map data, and the image data which shows a halftone image as image data for constituting one screen, The 1st output means which outputs the bit map data generated with said generating means, It is characterized by having the 2nd output means which carries out lossy compression of the staining data generated with said generating means, and outputs them, and the 3rd output means which carries out lossy compression of the image data generated with said generating means, and outputs it.
[0007] It is characterized by making it lower than the resolution as which the bit map data outputted by said 1st output means express the resolution which the staining data especially outputted by said 2nd output means express.
[0008]
[Embodiment of the Invention]
(Gestalt of the 1st operation) Drawing 1 (a) is the block diagram showing the configuration of the image storage section of the image processing system concerning the gestalt of operation of the 1st of this invention. As for gradation memory, and 6 and 53, for resolving memory and 50, a data discrimination decision circuit, and 4, 51 and 52 are [one / an input terminal and 3 / a selector and 7] output terminals among drawing.
[0009] As for the data which the host computer etc. is connected to the input terminal 1, and were inputted from the input terminal 1, header information is interpreted by the data discrimination decision circuit 50, and the image data to which, as for a background color, the gradation (color) data of a text have halftone in the gradation memory 51 at the gradation memory 4 is respectively stored in the resolving memory 3 for the bit map data of a text at the gradation memory 52. If the data for 1 page are transmitted to each above-mentioned memory from a host computer and printer engine is started, according to the synchronizing signal from a printer side, read-out of memory will be controlled so that the data corresponding to each pixel are outputted to order by the head of a page from the resolving memory 3 and the gradation memory 4, 51, and 52. The image field signal 122 which the output (namely, background color) of the gradation memory 51 is connected to the terminal a of a selector 53, and the output (namely, image data) 121 of the gradation memory 52 is connected to Terminal b, and is outputted to a control terminal from the gradation memory 52 is inputted. Therefore, when the present pixel is an image field, out of an image field, a background color is outputted for an image data to the terminal c of a selector 52 (the terminal b of a selector 6 is supplied).
[0010] According to the output data of the resolving memory 3, when the data of the resolving memory 3 are "1" and the data of the resolving memory 3 are "0" about the data (namely, data of the gradation memory 4) of Terminal a as a drawing color, a selector 6 chooses the data (namely, data of the gradation memory 5) of Terminal b as a background color, and outputs gradation data to printer engine from an output terminal 7.
[0011] The data stored in the resolving memory 3 are data for the gradation memory 4 and the change of

five, and are data of 1 bit of each pixel by this example for resolution maintenance.
[0012] On the other hand, although full gradation data (a total of 24-bit data [The gestalt of this operation] of 8 bits each of RGB) are respectively stored in the gradation memory 4 and 51, the number of pixels (resolution) is restricted for memory space reduction.
[0013] Drawing 2 is the block diagram showing the example of a concrete configuration of the gradation memory 52 of the gestalt of this operation. For memory and 54, as for a compression circuit and 56, a compressibility setting circuit and 55 are [nine / an expanding circuit and 57] field detectors among drawing.
[0014] The start address and the image area size, i.e., the width of face, and the height of an image field are set to the header of an image data, and from the width of face and the height of the above-mentioned image field, in quest of the amount of data of an image field, the compressibility setting circuit 54 sets up compressibility from a ratio with the capacity of memory 9, and outputs it to the compression circuit 55. The compression circuit 55 is a circuit as shown in drawing 3 , quantization conditions are controlled to become the set-up compressibility and compressed data is stored in memory 9. Moreover, in the compressibility setting circuit 54, from header information, the coordinate value of the starting point of an image field and a terminal point is also generated, and the above-mentioned coordinate value is set as each register of the field detector 57. The field detectors 57 are the field detector 33 of drawing 7 mentioned later, and same circuit.
[0015] On the other hand, synchronizing with HSYNC by the side of a printer, if printer engine is started, the field detector 57 will output an image field signal from a signal line 122, when the present pixel judges whether it is the pixel of an image field and judges with an image field. If an image field signal is inputted into the expanding circuit 56, the expanding circuit 56 will elongate the compressed data stored in memory 9 to the original image data, and will output it from a signal line 121.
[0016] The compression circuit 55 is a compression coding network which performs well-known coding of orthogonal transformation coding, vector quantization, block coding, etc. With the gestalt of this operation, for memory space reduction, since the compression ratio is set up quite highly, irreversible coding is used. Therefore, resolution is not saved. However, of course, reversible coding, such as run length coding, may be used.
[0017] Drawing 3 is the block diagram showing the example of a concrete configuration of the compression circuit 55. The gestalt of this operation is Baseline of the international-standards-ized proposal of color static-image coding proposed in JPEG (Joint Photographic Expert Group) which is the joint activity object of ISO and CCITT. The coding section of System is shown. (407 Bibliography: Yasuda, "formation of color still picture coding international standards", the Institute of Image Electronics Engineers of Japan, the 18th volume, No. 6, PP.398- 1989)
[0018] The image pixel data inputted from the signal line 103 are cut down 8x8 pixels in the shape of a block in the blocking circuit 11 constituted by the Rhine memory for several lines, cosine conversion is carried out in the discrete cosine transform (DCT) circuit 12, and a transform coefficient is supplied to a quantizer (Q) 13. In a quantizer 13, linear quantization of a transform coefficient is performed according to the quantization step information impressed on the quantization table 14. Among the quantized transform coefficients, difference (prediction error) with DC component of a pre-block is taken in the predicting-coding circuit (DPCM) 15, and DC multiplier is supplied to the Huffman coding circuit 16. Drawing 4 is the detailed block block diagram of the predicting-coding circuit 15. DC multiplier quantized from the quantizer 13 is impressed to a delay circuit 25 and a subtractor 216. A delay circuit 25 is a circuit delayed by the time amount which needs a discrete cosine transform circuit for 1 block, i.e., the operation for 8x8 pixels, therefore DC multiplier of a pre-block is supplied to a subtractor 26 from a delay circuit 25. Therefore, the difference (prediction error) of DC multiplier with a pre-block will be outputted to the output of a subtractor 26. (Since the pre-block value is used as a forecast, a prediction machine consists of these predicting coding like the above-mentioned in a delay circuit.)
[0019] The Huffman coding circuit 16 carries out variable length coding of the prediction error signal supplied from the predicting-coding circuit 15 according to DC Huffman code table 17, and supplies DC Huffman code to the multiplexing circuit 24.

[0020] On the other hand, as the scanning conversion circuit 18 shows to drawing 5 (a) from the multiplier of a low degree, the zigzag scan of the AC multiplier (multipliers other than DC multiplier) quantized with the quantizer 13 is carried out at order, and it is supplied to the capable multiplier detector 19. Quantized AC multiplier judges whether it is "0", in the case of "0", a count-up signal is supplied to the run length counter 20, and it makes the value of a counter increase +one time in the capable multiplier detector 19. On the other hand, in the case of multipliers other than "0", a reset signal is supplied to a run length counter, while resetting the value of a counter, a multiplier is divided into group number SSSS and an overhead bit as shown to drawing 5 (b) by the grouping circuit 21, group number SSSS is supplied to the Huffman coding circuit 22, and an overhead bit is respectively supplied to the multiplexing circuit 24. The run length counter 20 supplies the number NNNN of "0" between capable multipliers other than "0" to the Huffman coding circuit 22 in the circuit which counts the run length of "0." The Huffman coding circuit 22 carries out variable length coding of the group number SSSS of a capable multiplier to the run length NNNN of supplied "0" according to AC Huffman code table 23, and supplies AC Huffman code to the multiplexing circuit 24.
[0021] In the multiplexing circuit 24, DC Huffman code, AC Huffman code, and the overhead bit for 1 block (input pixel of 8x8) are multiplexed, and the image data compressed from the signal line 104 is outputted.
[0022] Therefore, the compressed data outputted from a signal line 104 is memorized in memory, and reduction of memory space is possible for the time of above-mentioned compression at the time of read-out by elongating by reverse actuation.
[0023] In addition, since the expanding circuit 56 performs the twist operations of the compression circuit 8, explanation is omitted.
[0024] Drawing 6 is the block diagram showing the concrete example of a configuration of the gradation memory 4 and 51. As for a selector and 30, 29 and 31 are [a register group and 32] field judging circuits among drawing.
[0025] Sequential storing of the gradation data inputted from the signal line 108 is carried out by the selector 29 from a register 30-2 to 30-n. In addition, default gradation data (for example, the gradation memory 4 white and the gradation memory 51 white) are set to the register 30-1. The field judging circuit 32 judges the range where the gradation data stored in each register become effective from the coordinate value of the output data of the resolving memory 3 inputted from a signal line 105,106, controls a selector 31, and outputs effective gradation data from a signal line 109.
[0026] Drawing 7 is the block diagram showing the concrete example of a configuration of the field judging circuit 32. As for a register, and 39 and 40, for a field detector and 34, a priority encoder, and 35, 36, 37 and 38 are [33 / a comparator circuit and 41] AND circuits among drawing.
[0027] With the gestalt of this operation, it limits to a rectangle as shows the service area of each gradation register 30-2 - 30-n to drawing 8 , and sets up by two of the points (x1, y1) (a "terminal point" is called a rectangular lower right corner and the following among drawing) scanned by the point (x0, y0) (the "starting point" is called the rectangular upper-left-hand-corner section and the following among drawing 8) scanned first, and the last. In addition, the direction of the x axis in drawing is made into the main scanning direction of a printer, and the direction of the y-axis is made into the direction of vertical scanning. the coordinate value (x0, y0) of the above-mentioned starting point identified from the data discrimination decision circuit 2 and a terminal point, and (x1, y1) are stored in the each registers 35, 37, 36, and 38 of the field detector 33 corresponding to the gradation register 30 of drawing 6 .
[0028] On the other hand, at the time of print-out, each coordinate value of the pixel data read from the resolving memory 3 is inputted from a signal line 105,106. The 1st comparator circuit 39 compares the x-coordinate value x of the above-mentioned resolving memory 3 with the x-coordinate values x0 and x1 of the starting point and x terminal points, and inputs "0" into AND circuit 41 for "1" at the time of $x<x0$ or $x>x1$ at the time of $x0 <= x <= x1$. The 2nd comparator circuit 40 inputs "0" into AND circuit 41 for "1" similarly at the time of $y<y0$ or $y>y1$ at the time of $y0 <= y <= y1$. Therefore, "0" is outputted at the times other than "1", and (ii) and (i) at the time of (i) $x0 <= x <= x1$ and $y0 <= y <= y1$, and field detection is attained from AND circuit 41. By the priority encoder 34, the number of the field set as the

last among the detected fields is encoded, and the result detected in each field detector 33-2 - 33-n is outputted from a signal line 107, in order to perform the priority judging of a duplication part as shown in the slash section of drawing 8 . That is, in a duplication part, it is judged with the field set up later being effective. In addition, when each field judging results of all are set to "0", a priority encoder 34 outputs "0" and controls a selector 31 to choose the gradation data (namely, default) of the gradation register 30-1 of drawing 6 .

[0029] Usually, the dot resolving data with which high resolutions, such as a text, are demanded are stored in the resolving memory 3, and the data with which the Takashina tonality, such as an image, is demanded are stored in the gradation memory 5. The gradation (color) data of text data are stored in the gradation memory 4. When the text data to which the case of regularity (namely, monochrome) or a background (background color) laps [the gradation (color) of text data] with the image section in regularity (monochrome) over 1 page is the above-mentioned background color, since the contents of the above and the gradation memory 4 serve as only a default, they become unnecessary [the register after said field judging circuit 32 and 30-2].

[0030] In addition, a configuration which carries out 1 gradation (color) setup per block of 8 (pixel)x8 (Rhine) is sufficient as gradation memory.

[0031] Although the resolving memory 3 is memory which has the capacity for a page by 1 bit of each pixel, since it is used for the change of gradation data, the correlation between pixels is quite high and compression of the amount of data is also possible by using reversible data compression coding as shown in drawing 12 .

[0032] Drawing 12 is the block diagram showing the gestalt of other operations of the resolving memory 3. For a run-length-coding circuit and 61, as for memory and 63, a Huffman coding circuit and 62 are [60 / the Huffman decryption circuit and 64] run length decryption circuits among drawing. Since it is well-known about a run length, and Huffman coding and a decryption circuit, explanation is omitted.

[0033] Drawing 1 (b) is drawing containing the image storage section of drawing 1 (a) showing the whole image processing system configuration.

[0034] In drawing 1 (b), although 200 is the image input section connected with the host computer, you may be the interface of external instruments, such as image readers, such as an image scanner containing a CCD sensor, and SV camera, a video camera, etc. In the case of the latter, in the data discrimination decision circuit 50, it is made to identify the above-mentioned data. The image data inputted from 200 is supplied to the input terminal 1 of the image storage section 201 shown in drawing 1 (a). The control unit to which, as for 202, an operator performs assignment of the output destination change of image data etc., and 203 are the output-control sections, and perform the output of the synchronizing signal of memory read-out, such as selection of the output destination change of image data, and HSYNC of printer engine, etc. A synchronizing signal is supplied to the discrimination decision circuit 50 and each memory of drawing 1 (a), and is used as control signals, such as read-out from a data transfer and memory. The transmitting section which 204 minds the image display sections, such as a display, and 205 minds a public line and a Local Area Network, and communicates image data, and 206 are the image output sections, such as a laser beam printer which irradiates a laser beam, forms a latent image for example, on a photo conductor, and visible-image-izes this. In addition, the image output sections 206 may be an ink jet printer, a thermal transfer printer, a dot impact printer, etc.

[0035] As mentioned above, the image memory which the gestalt of this operation compresses continuous tone data, such as an image data, using the correlation between pixels, and a vision property, and is memorized, The gradation memory which memorizes a text color (drawing color) or a background color for every specific region, Reduction of memory space is aimed at keeping good the image quality of both a text and an image by preparing the resolving memory which saves the dot resolution of pixel data, and switching the output data of the above-mentioned image memory and gradation memory according to the output signal of this resolving memory.

[0036] (Gestalt of the 2nd operation) Drawing 9 is the block diagram showing the configuration of the image processing system concerning the gestalt of operation of the 2nd of this invention. The same coding is given to the component which achieves the same function as drawing 1 among drawing, and

only a different point from the gestalt of operation of drawing 1 is explained hereafter.
[0037] It is 2 bundle data discrimination decision circuit among drawing. As for the data inputted from the input terminal 1, header information is interpreted in the data discrimination decision circuit 44, a drawing color [in / to the resolving memory 3 / in the resolving data for background discernment / a background color and an image field] is stored in the gradation memory 4, and the drawing color and image data of a text are respectively stored in the gradation memory 52. If the data for 1 page are transmitted to each above-mentioned memory 3, 4, and 52 and printer engine is started, from the resolving memory 3 and the gradation memory 4 and 52, the data corresponding to each pixel will be respectively supplied to the control terminal of a selector 6, Terminal a, and Terminal b one by one from the head pixel of a page by the synchronizing signal. A selector 6 outputs gradation data for the background color which is the output of the gradation memory 4, the drawing color of the text which is the output of the gradation memory 52, and an image data to printer engine from a change and an output terminal 7 according to the output signal of the resolving memory 3.
[0038] It consists of gestalten of this operation so that the resolution of a background may be saved. Usually, to the drawing color number of a text, since it is very few, the hard amount of the gradation memory 4 can do the background color number in 1 page quite small. Moreover, by the gestalt of the 1st operation, when the drawing color of a text changes continuously (in the name case [For example, the gradation and the coordinate of an alphabetic character were shifted little by little, and carried out overwrite. it needs.]), although false gradation processing of a dither etc. is actually needed, with the gestalt of this operation, very good image quality is acquired by storing said drawing color in the gradation memory 5 advantageous to storage of a continuous tone. Moreover, since it consists of gestalten of this operation so that the resolving power of a background may be saved, trimming of the image section can be easily performed by the maximum resolution of a printer.
[0039] (Gestalt of the 3rd operation) Drawing 10 is the block diagram showing the configuration of the image-processing store concerning the gestalt of operation of the 3rd of this invention. The same sign is given to the component which achieves the same function as drawing 1 among drawing, and only a different point from the gestalt of operation of drawing 1 is explained hereafter.
[0040] As for a data discrimination decision circuit and 45, 44 are [a field judging circuit and 46] EXOR circuits among drawing.
[0041] As for the data inputted from the input terminal 1, header information is interpreted in the data discrimination decision circuit 44, a drawing color [in / to the resolving memory 3 / in the bit map data of a background / a background color and an image field] is stored in the gradation memory 4, and the drawing color and image data of a text are respectively stored in the gradation memory 52. Moreover, an image field is stored in the register of the field judging circuit 45. The data for 1 page are transmitted to each above-mentioned memory 3, 4, and 52 from a host computer, and if printer engine is started, from the resolving memory 3, the gradation memory 4 and 52, and the field judging circuit 45, the data corresponding to each pixel will be outputted one by one from the head pixel of a page. The field judging circuit 45 supplies "1" to one terminal of the EXOR circuit 46, when the present pixel is an image data. The output of the resolving memory 3 is connected to another terminal of the EXOR circuit 46, and the resolving data in an image field are reversed by the above-mentioned configuration. Therefore, as for a selector 6, in the case of the text pixel in a background and an image field, the gradation data which outputted the gradation (color) data of a terminal b 5, i.e., gradation memory, from Terminal c except the above, and were chosen from the output terminal 7 are supplied to printer engine in the gradation (color) data of a terminal a 4, i.e., gradation memory.
[0042] With the gestalt of this operation, since the contents of resolving memory are reversed in the image section, overwrite of text data can perform easily. That is, process the text data which carries out overwrite to the above-mentioned image section with a host computer as background data with the gestalt of the 2nd operation. That is, with the gestalt of this operation, although it is necessary in "1" to store "0" in addition to the above, only the image section by which overwrite of the text is not carried out to the resolving memory 3, and the text drawing section outside an image field should always set the text drawing section as "1" irrespective of the inside and outside of an image field in order to reverse the

output of the resolving memory 3 in an image field.
[0043] In addition, although resolving memory was constituted from 1 bit of each pixel in the gestalt of the 1st - the 3rd operation, this invention is good also as a configuration which chooses gradation data from four kinds of gradation memory as 2 bits not only of this but each pixel.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing the image processing system of the gestalt of the 1st operation
[Drawing 2] Drawing showing the example of a concrete configuration of a gradation memorandum value
[Drawing 3] Drawing showing the example of a concrete configuration of a compression circuit
[Drawing 4] Drawing showing the example of a concrete configuration of a predicting-coding circuit
[Drawing 5] Drawing showing the scanning sequence of a DCT multiplier
[Drawing 6] Drawing showing the example of a concrete configuration of the 2nd gradation memory
[Drawing 7] Drawing showing the example of a concrete configuration of a field judging circuit
[Drawing 8] Drawing showing the service area of the gradation memory on a page
[Drawing 9] Drawing showing the 2nd configuration of the gestalt of operation
[Drawing 10] Drawing showing the 3rd configuration of the gestalt of operation
[Drawing 11] Drawing showing the example of a concrete configuration of the 3rd gradation memory
[Drawing 12] Drawing showing other examples of a concrete configuration of resolving memory
[Description of Notations]
2, 44, 50 Data discrimination decision circuit
3 Resolving Memory
4, 51, 52 Gradation memory
6 53 Selector
45 Field Judging Circuit
46 EXOR Circuit

[Translation done.]

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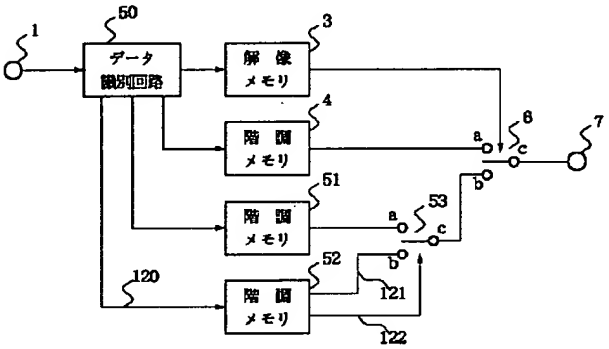
3.In the drawings, any words are not translated.

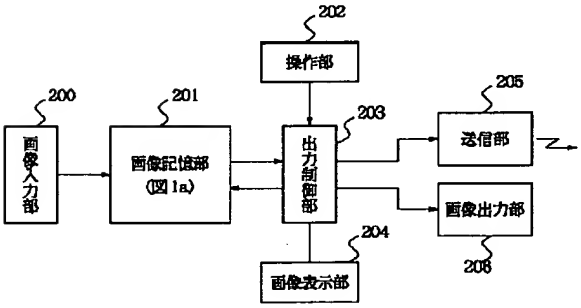
DRAWINGS

[Drawing 1]

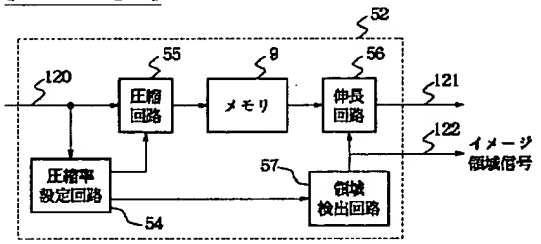
(a)



(b)



[Drawing 2]



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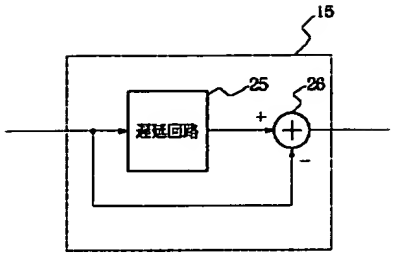
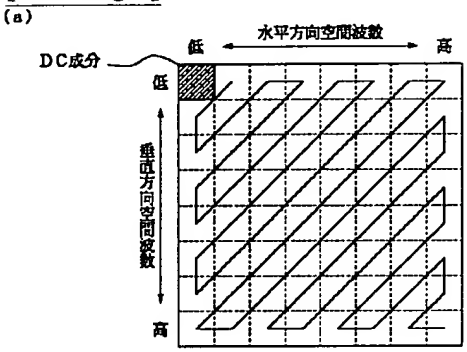
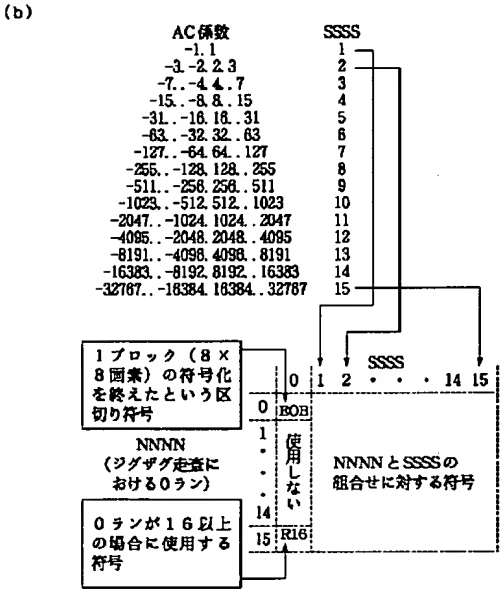
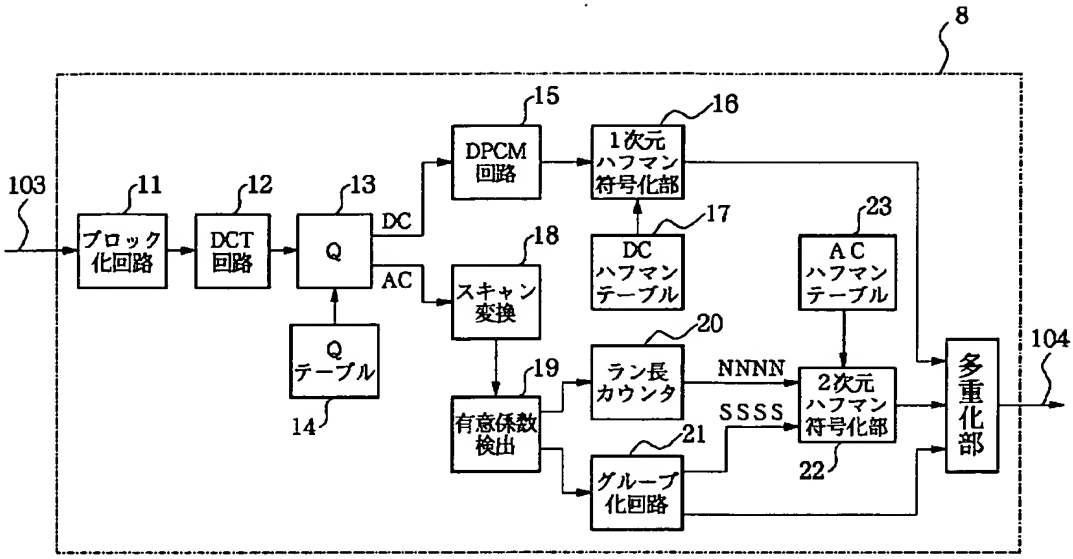


[Drawing 5]

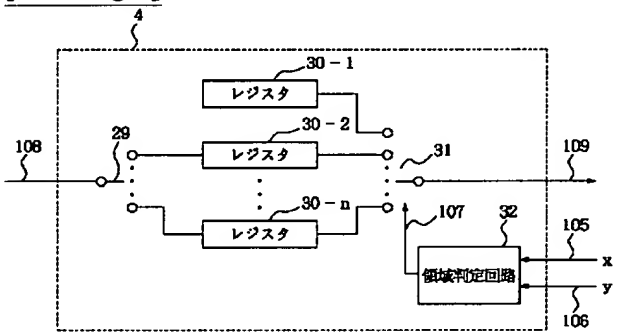




[Drawing 3]



[Drawing 6]



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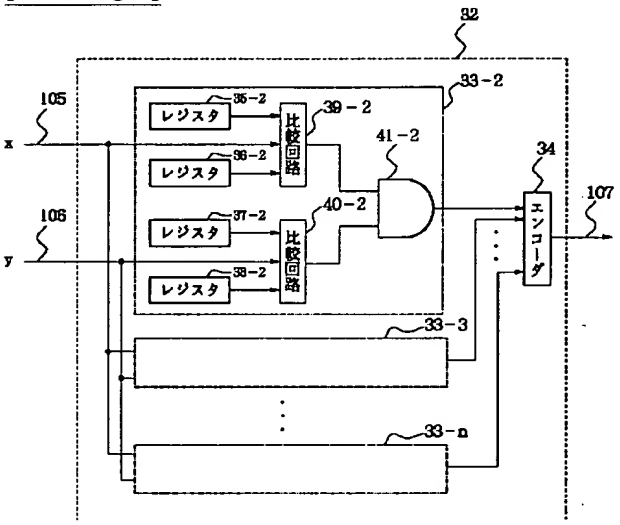
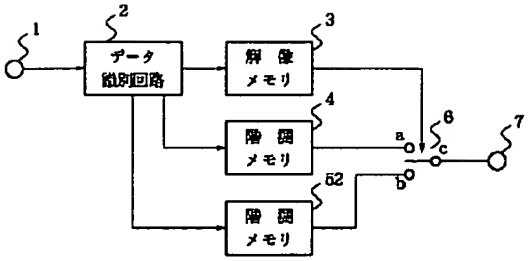


[Drawing 9]



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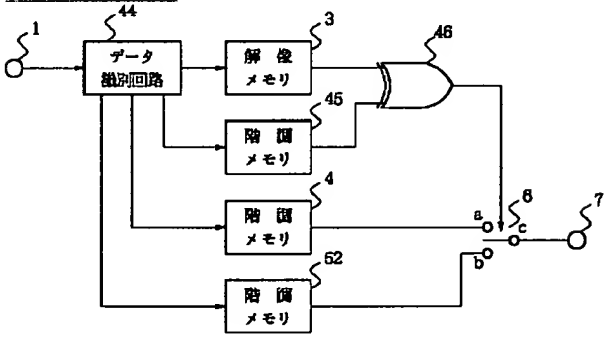

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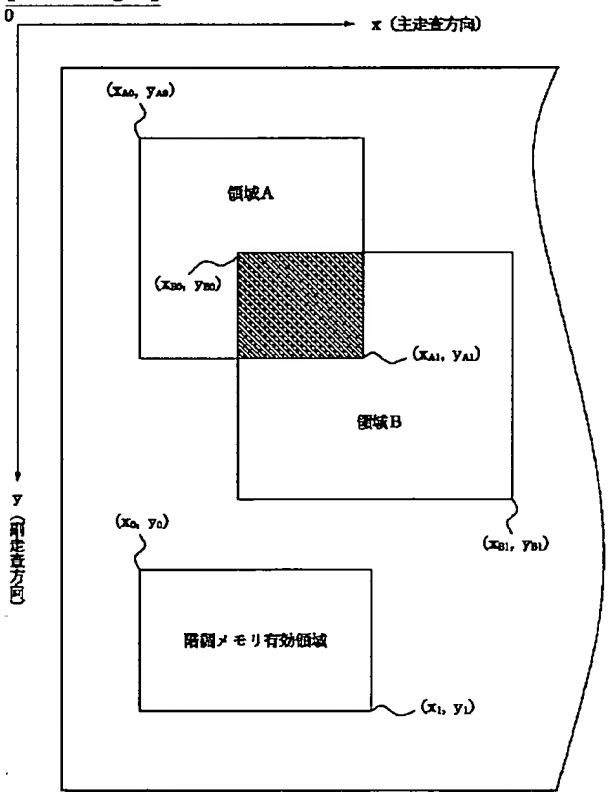
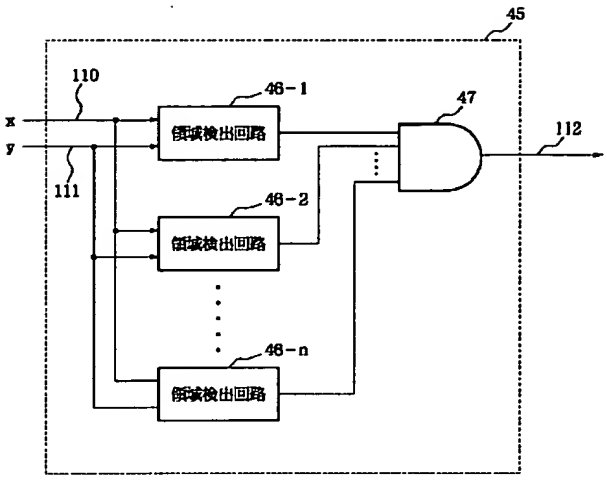
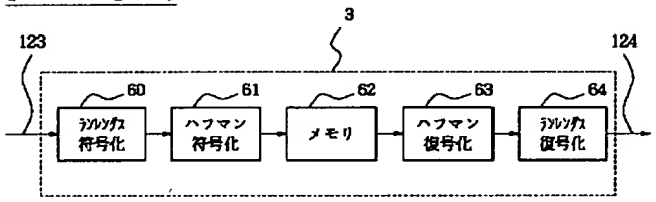


[Drawing 11]



[Drawing 12]



[Translation done.]